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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,106	12/23/2003	Uwe Nagel	Q78542	8008

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EXAMINER	
HOLTON, STEVEN E	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,106	NAGEL, UWE	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 10-12* is/are rejected.

7)☒ Claim(s) *7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (USPN: 6597370) in view of Choi (USPN: 6404422).

Regarding claims 1, 10, 11, and 12, the claims are drawn to a associated methods of operation and associated display devices, Lee discloses a method for adjusting the scanning phase of an analog/digital converter for an image reproducing device with a method of operation including, “applying the analog video signal to the image reproducing (Fig. 2, the input R,G,B analog signal is applied to the LCD module, element 70), comparing the digital image data buffered in the image memory (Fig. 2, element 60) with predefined data (Fig. 2, element 20 stores the predefined data) that corresponds to the analog video signal (col. 4, lines 7-67; lines 50-67 particularly discuss comparing reference data with sampled data to determine a difference between signals)". Lee further discloses changing the scanning phase of the scanning clock based that is used for scanning in the analog display data (col. 4, lines 50-67) this is performed so that the predefined data and the input data are made to match (Fig. 3, shows the flow chart of testing the data and changing the scanning phase until the data matches).

However, Lee does not disclose adjusting the scanning frequency. Lee only discusses adjusting the phase of the scanning clock that is output by the phase locked loop (Fig. 2, element 30, the PLL).

Choi discloses a display device and method for controlling a liquid crystal display device that includes adjusting the phase and frequency of a phase locked loop used to operate an analog-to-digital converter (abstract; col. 5, lines 11-16). Fig. 2 shows the system of Choi where an analog image signal is input into an A/D converter, scanned using the frequency of the PLL circuit section and then calculations of the data are performed that allow for adjustment of the phase and frequency of the output of the PLL circuit section.

At the time of invention it would have been obvious to modify the teachings of Lee with the teachings of Choi. The system of Lee which is able to adjust the phase of the phase locked loop timing circuit could be modified based on the teachings of Choi so that both the phase and frequency of the PLL circuit could be adjusted. The motivation would be to produce a system that could automatically adjust the screen status of a display device by properly adjusting and shifting the phase and frequency of input analog signal (Choi, col. 1, lines 51-56). Thus, it would have been obvious to modify the teachings of Lee with the teachings of Choi to produce a system that compares an input signal with a predetermined reference signal so that the scanning frequency and phase of an analog-to-digital converter could be adjusted so that the scanned image data matches the inputted analog data.

2. Claims 2-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Choi as applied to claim 1 above, and further in view of Naka et al. (USPN: 5990968), hereinafter Naka.

Regarding claim 2, Lee discloses extracting a specific area from the input image data to compare to a respective area of the reference image data (col. 4, lines 50-56; the predetermined area). The predetermined area used by Lee for comparing the input data with the reference data would be a marking of some sort for use in the comparison. Lee does not expressly disclose where the marking is provided, but it would be a matter of design choice for one of ordinary skill in the art to choose the predetermined area to be on the right edge of the image data, the left edge of the image data, or any other predetermined area within the image data.

The combination of Lee and Choi do not expressly disclose the limitation, "wherein the analog video signal corresponds to a test image that has a regular pattern in horizontal direction".

Naka discloses a method of adjusting the phase of a sampling clock for an analog-to-digital filter that involves providing a test signal for consideration and adjustment of the sampling clock. The test signal for use in the measurement is made having black and white signals of predetermined levels including variations between the levels occurring frequently (col. 6, lines 48-54). It would have been a matter of design choice for one of ordinary skill in the art to use a pattern that changes in the horizontal direction or the vertical direction. Horizontally changing test patterns are known for adjusting display devices.

At the time of invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Lee and Choi with the teachings of Naka. The methods of adjusting the phase and frequency of a sampling clock of an analog-to-digital converter disclosed by Lee and Choi could be combined with the test signal described by Naka having a frequently changing black and white signal. The motivation for doing so would be to produce a system to automatically adjust a sampling phase easily and with more precision (Naka, col. 2, lines 41-43). Thus, it would have been obvious to one of ordinary skill in the art to combine the teachings of Lee, Choi, and Naka to produce a method of adjusting the scanning frequency and phase of an analog-to-digital converter in an image display system as described in claim 2.

Regarding claim 3, Naka discloses the test pattern comprises different brightness values (col. 6, lines 48-54). The predetermined area of Lee could comprise any specific selection of the test pattern described by Naka. By selecting a section of the display with multiple changes between white and black, the marking could comprise multiple pixels with white values and multiple pixels with black values.

Regarding claim 4, Naka discloses the brightness values of the pixels vary by a maximum value of black to white (col. 6, lines 48-54).

Regarding claim 5, all of the displays of Lee, Choi, and Naka have a predetermined resolution and it would be obvious to one of ordinary skill in the art to select a test pattern that is adapted to the resolution of the display device. Lee further uses a scaling device (Fig. 2, element 50) to adjust the input testing signal so that it correctly matches the resolution of the display device (col. 4, lines 23-32). Thus, it

would have been obvious to one or ordinary skill in the art to use a scaler to adjust the test pattern to match a predetermined resolution or to input a test pattern that requires no resolution change.

Regarding claim 6, Naka discloses a test pattern with a changing dot pattern (Figs. 3A-3C show an input signal, the dot clock/sampling clock and correctly outputted display information). The changing test pattern based on a dot clock frequency represents multiple pixels transmitted in order for display. Thus, Naka discloses that a predetermined number of consecutive pixels are checked against predefined data (Figs. 4A and 4B show comparisons between the expected results and the sampled output). Lee further discloses testing a predetermined area of the input data against the test data. It would have been a matter of design choice to choose the predetermined area to be a group of consecutive pixels at the beginning of a line, the end of a line, or some other selected group of pixels within the input data.

Regarding claim 8, Lee discloses comparing a predetermined area with the predefined test pattern to determine if they match (col. 4, lines 50-56).

Allowable Subject Matter

3. Claims 7 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The present invention is directed to a method of adjusting the scanning frequency and phase of an analog-to-digital converter for use with a display device.

Claim 7 identifies the uniquely distinct features increasing the scanning phase to determine a first boundary value, resetting the phase and then decreasing the phase to determine a second boundary and adjusting the scanning phase based on the average value of the first and second boundary values. The closest prior art, Naka, Lee, and Choi disclose methods of adjusting the phase of the scanning signal including either increasing or decreasing the phase to determine an optimum level, but fail to determine the correct phase based on an average of two boundary readings, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoo (USPN: 7236163) discloses a method adjusting the phase of an analog-to-digital converter associated with a display panel. Zeidler (USPN: 6734898) discloses comparing input image data with reference data for correction of other types of display errors. Wilensky et al. (USPN: 4466014) shows a variety of test images to be used for testing of a display device and discusses that other test images could be created depending on the display factors to be tested.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571)272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven E. Holton
Division 2629
June 20, 2008

/Richard Hjerpe/
Supervisory Patent Examiner, Art Unit 2629